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EXAMINER	
SPITTLE, MATTHEW D	

ART UNIT	PAPER NUMBER
2111	

DATE MAILED: 02/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/829,187	SHAVER, CHARLES N.	
	Examiner	Art Unit	
	Matthew D. Spittle	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 February 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,10-17 and 20-26* is/are rejected.

7)☒ Claim(s) *8,9,18 and 19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/22/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Intel Corporation.

With regard to claim 1, Intel Corporation teach an expansion card for adding to a computer system a Universal Serial Bus (USB) port comprising:

An Accelerated Graphics Port (AGP) card connector configured to enable the expansion card to be inserted into an expansion slot of the computer system (Page 188, Section 4.3.12);

Intel Corporation fail to explicitly teach at least one USB port each adapted to mate with a USB-compatible peripheral device, and wherein a USB data signal is received at the AGP connector and routed to the USB port.

Examiner takes official notice that it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to add USB ports to the AGP expansion card for the purposes of connecting a USB device to it since USB signals are present in an AGP card slot (page 231, pins: 4B, 4A).

Examiner takes official notice that it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to route the USB data signals received at the AGP connector the USB port. This would have been obvious since without doing so, the USB port would not be functional.

* * *

Claims 2, 4, 5, 7, and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Intel Corporation in view of USBIF.

With regard to claim 2, Intel Corporation fail to teach the expansion card of claim 1 wherein one or more of the at least one USB port is a USB-Plus-Power port comprising a USB receptacle at which a USB data signal and a USB power signal are presented, and a power receptacle at which a power signal is presented to a mated USB-compatible peripheral device.

USBIF teach a USB-Plus-Power port comprising a USB receptacle (Page 18, Figures 8, 9) at which a USB data signal and a USB power signal are presented, and a power receptacle at which a power signal is presented to a mated USB-compatible peripheral device (page 16 teaches the data signals and power signals in section 3.1.3.4).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to incorporate a USB-Plus-Power port as taught by USBIF for the purpose of supplying power to a USB device. This would have been obvious in order to eliminate the need for an external power supply to power the USB device.

With regard to claim 4, Intel Corporation implicitly teach the additional limitation wherein the expansion card further comprises:

A power connector, matable with a corresponding power connector of the computer system, through which the power signal is received (Intel Corporation teach an AGP add-in card, which contains a power connector in the slot connector; namely pins A1, B2, B3, B5, B9, A9, and several others that provide voltages). Examiner takes official notice that it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to route the power signals to the at least one or more of the USB-Plus-Power ports. This would have been obvious since without doing so, the USB-Plus-Power port would not provide power to the attached device.

With regard to claim 5, Intel Corporation implicitly teach the additional limitation wherein the additional power signal is a 12VDC power signal. This is evidenced by the page 231, Table 5-2 which lists a 12VDC power signal on pin A1.

With regard to claim 7, USBIF teaches the additional limitation of a 24VDC power signal routed to one or more of the at least one USB-Plus-Power ports (page 8, section 3.1), but fail to explicitly teach a circuit configured to convert the 12VDC power signal to a 24VDC power signal. Examiner takes official notice that voltage-doubling circuits are old, and well known in this art. Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to utilize a voltage-doubling circuit in the expansion card of Intel Corporation, and USBIF for the purpose of providing the 24VDC in a USB port as required by the USB-Plus-Power specification.

With regard to claim 8, USBIF teaches the additional limitation of USB-Plus-Power ports. It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to utilize USB-Plus-Power ports as taught by USBIF for the purpose of supplying power to a USB device. This would have been obvious in order to eliminate the need for an external power supply to power the USB device.

* * *

Claim 3 is rejected under 35 U.S.C. 103(a) as being obvious Intel Corporation, and further in view of Lelong et al. .

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art only under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 103(a) might be overcome by: (1) a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not an invention "by another"; (2) a showing of a date of invention for the claimed subject matter of the application which corresponds to subject matter disclosed but not claimed in the reference, prior to the effective U.S. filing date of the reference under 37 CFR 1.131; or (3) an oath or declaration under 37 CFR 1.130 stating that the application and reference are currently owned by the same party and that the inventor named in the application is the prior inventor under 35 U.S.C. 104, together with a terminal disclaimer in accordance with 37 CFR 1.321(c). This rejection might also be overcome by showing that the reference is disqualified under 35 U.S.C. 103(c) as prior art in a rejection under 35 U.S.C. 103(a). See MPEP § 706.02(l)(1) and § 706.02(l)(2). .

With regard to claim 3, Intel Corporation fail to teach a USB connector, matable with a corresponding USB connector of the computer system, at which at least one additional USB data signal and at least one USB power signal generated by the computer system are received, wherein each of the additional USB data signal and USB power signal is routed to one or more of the at least one USB port.

Lelong et al. teach a USB connector (Figure 2, item 103), matable with a corresponding USB connector of the computer system (Figure 2, labeled "USB header"; Figure 1, item 15), at which at least one additional USB data signal and at least one USB power signal generated by the computer system are received, wherein each of the additional USB data signal and USB power signal is routed to one or more of the at least one USB port (paragraph 39).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to incorporate the USB connector as taught by Lelong et al. into the expansion card of Intel Corporation. This would have been obvious in order to allow the USB ports provided on the expansion card to be controlled by a USB controller incorporated into the computer system motherboard.

* * *

Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Intel Corporation, in view of USBIF, and further in view of Espenshade et al.

With regard to claim 6, Intel Corporation, and USBIF fail to teach the expansion card further comprising at least one circuit each associated with one of the at least one USB port, wherein each circuit performs signal conditioning operations on at least one signal provided at its associated USB port.

Espenshade et al. teach a USB connector that comprises a circuit that performs signal conditioning operations on at least one signal provided at its associated USB port (column 2, lines 9 – 15).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to include the signal conditioning USB connector of Espenshade et al. in the expansion card of Intel Corporation, and USBIF. This would have been obvious since Espenshade et al. teach that the signal conditioning components within their USB connector eliminates undesirable extraneous signals such as high frequency noises (column 4, lines 25 – 28).

* * *

Claims 11 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Intel Corporation.

With regard to claim 11, Intel Corporation teach an expansion comprising:

A plurality of connectors through which USB data, USB power, and power signals are received (page 231, pins 4B, 4A, 1A, 5A, 5B, 9A, 9B), wherein each connector is matable with a corresponding connector of the computer system (where Examiner interprets the connectors as each individual pin of the AGP slot connector on the AGP expansion card, and the corresponding connectors in the AGP slot in the computer system).

Examiner takes official notice that it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to add a plurality of USB ports to the AGP expansion card for the purposes of connecting a USB device to it since USB signals are present in an AGP card slot (page 231, pins: 4B, 4A).

Intel Corporation fail to explicitly teach at least one USB port each adapted to mate with a USB-compatible peripheral device, and wherein a USB data signal is received at the AGP connector and routed to the USB port.

Examiner takes official notice that it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to include circuitry routing the USB data, USB power and power signals from the plurality of connectors to the USB ports. This would have been obvious since without doing so, the USB port would not be functional.

One of the plurality of connectors is an Accelerated Graphics Port (AGP) card connector configured to enable the expansion card to be inserted into an AGP expansion slot of the computer system (page 188, section 4.3.12).

With regard to claim 15, Intel Corporation implicitly teaches the additional limitation wherein the additional power signal is a 12VDC power signal. This is evidenced by the page 231, Table 5-2 which lists a 12VDC power signal on pin A1.

* * *

Claims 12, 14, and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable Intel Corporation in view of USBIF.

With regard to claim 12, Intel Corporation fail to teach the expansion card of claim 11 wherein one or more of the at least one USB port is a USB-Plus-Power port comprising a USB receptacle at which a USB data signal and a USB power signal are presented, and a power receptacle at which a power signal is presented.

USBIF teach a USB-Plus-Power port comprising a USB receptacle (Page 18, Figures 8, 9) at which a USB data signal and a USB power signal are presented, and a power receptacle at which a power signal is presented to a mated USB-compatible peripheral device (page 16 teaches the data signals and power signals in section 3.1.3.4).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to incorporate a USB-Plus-Power port as taught by USBIF for the purpose of supplying power to a USB device. This would have been obvious in order to eliminate the need for an external power supply to power the USB device.

With regard to claim 14, Intel Corporation implicitly teach the additional limitation wherein the expansion card further comprises:

A power connector, matable with a corresponding power connector of the computer system, through which the power signal is received (Intel Corporation teach

an AGP add-in card, which contains a power connector in the slot connector; namely pins A1, B2, B3, B5, B9, A9, and several others that provide voltages).

With regard to claim 17, USBIF teaches the additional limitation of a 24VDC power signal routed to one or more of the at least one USB-Plus-Power ports (page 8, section 3.1), but fail to explicitly teach a circuit configured to convert the 12VDC power signal to a 24VDC power signal. Examiner takes official notice that voltage-doubling circuits are old, and well known in this art. Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to utilize a voltage-doubling circuit in the expansion card of Intel Corporation, and USBIF for the purpose of providing the 24VDC in a USB port as required by the USB-Plus-Power specification.

* * *

Claim 13 is rejected under 35 U.S.C. 103(a) as being obvious over Intel Corporation in view of Lelong et al. .

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art only under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 103(a) might be overcome by: (1) a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not an

invention "by another"; (2) a showing of a date of invention for the claimed subject matter of the application which corresponds to subject matter disclosed but not claimed in the reference, prior to the effective U.S. filing date of the reference under 37 CFR 1.131; or (3) an oath or declaration under 37 CFR 1.130 stating that the application and reference are currently owned by the same party and that the inventor named in the application is the prior inventor under 35 U.S.C. 104, together with a terminal disclaimer in accordance with 37 CFR 1.321(c). This rejection might also be overcome by showing that the reference is disqualified under 35 U.S.C. 103(c) as prior art in a rejection under 35 U.S.C. 103(a). See MPEP § 706.02(l)(1) and § 706.02(l)(2). .

With regard to claim 13, Intel Corporation fail to teach a USB connector, matable with a corresponding USB connector of the computer system, at which at least one additional USB data signal and at least one USB power signal generated by the computer system are received, wherein each of the additional USB data signal and USB power signal is routed to one or more of the at least one USB port.

Lelong et al. teach a USB connector (Figure 2, item 103), matable with a corresponding USB connector of the computer system (Figure 2, labeled "USB header"; Figure 1, item 15), at which at least one additional USB data signal and at least one USB power signal generated by the computer system are received, wherein each of the additional USB data signal and USB power signal is routed to one or more of the at least one USB port (paragraph 39).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to incorporate the USB connector as taught by Lelong et al. into

the expansion card of Intel Corporation. This would have been obvious in order to allow the USB ports provided on the expansion card to be controlled by a USB controller incorporated into the computer system motherboard.

* * *

Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Intel Corporation, in view of USBIF, and further in view of Espenshade et al.

With regard to claim 6, Intel Corporation, and USBIF fail to teach the expansion card further comprising at least one circuit each associated with one of the at least one USB port, wherein each circuit performs signal conditioning operations on at least one signal provided to at least one of the plurality of USB ports.

Espenshade et al. teach a USB connector that comprises a circuit that performs signal conditioning operations on at least one signal provided at its associated USB port (column 2, lines 9 – 15).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to include the signal conditioning USB connector of Espenshade et al. in the expansion card of Intel Corporation, and USBIF. This would have been obvious since Espenshade et al. teach that the signal conditioning components within their USB connector eliminates undesirable extraneous signals such as high frequency noises (column 4, lines 25 – 28).

* * *

Claims 20 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Intel Corporation in view of USBIF.

With regard to claim 20, Intel Corporation teach an expansion card comprising:

A plurality of connectors for receiving USB data, USB power, and additional power signals (page 231, pins 4B, 4A, 1A, 5A, 5B, 9A, 9B; where Examiner interprets the connectors as each individual pin of the AGP slot connector on the AGP expansion card, and the corresponding connectors in the AGP slot in the computer system), comprising an Accelerated Graphics Port (AGP) card connector configured to enable the expansion card to be inserted into an AGP expansion slot of the computer system (page 188, Section 4.3.12 describes an AGP add-in card)

USBIF teach at least one Universal Serial Bus (USB)-Plus-Power port each adapted to mate with a USB-compatible device.

Examiner takes official notice that it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to route the USB data signals, USB power, and additional power signals received at the plurality connectors to the USB-Plus-Power port. This would have been obvious since without doing so, the USB-Plus-Power port would not be functional.

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to incorporate a USB-Plus-Power port as taught by USBIF for the

purpose of supplying power to a USB device. This would have been obvious in order to eliminate the need for an external power supply to power the USB device.

With regard to claim 21, Intel Corporation fails to teach the expansion card of claim 20 wherein one or more of the at least one USB-Plus-Power port comprises a USB receptacle at which a USB data signal and a USB power signal are presented, and a power receptacle at which a power signal is presented.

USBIF teach a USB-Plus-Power port comprising a USB receptacle (Page 18, Figures 8, 9) at which a USB data signal and a USB power signal are presented, and a power receptacle at which a power signal is presented to a mated USB-compatible peripheral device (page 16 teaches the data signals and power signals in section 3.1.3.4).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to incorporate a USB-Plus-Power port as taught by USBIF for the purpose of supplying power to a USB device. This would have been obvious in order to eliminate the need for an external power supply to power the USB device.

* * *

Claims 22 – 24, and 26 are rejected under 35 U.S.C. 103(a) as being obvious over Intel Corporation, in view of USBIF and further in view of Lelong et al. .

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art only under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 103(a) might be overcome by: (1) a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not an invention "by another"; (2) a showing of a date of invention for the claimed subject matter of the application which corresponds to subject matter disclosed but not claimed in the reference, prior to the effective U.S. filing date of the reference under 37 CFR 1.131; or (3) an oath or declaration under 37 CFR 1.130 stating that the application and reference are currently owned by the same party and that the inventor named in the application is the prior inventor under 35 U.S.C. 104, together with a terminal disclaimer in accordance with 37 CFR 1.321(c). This rejection might also be overcome by showing that the reference is disqualified under 35 U.S.C. 103(c) as prior art in a rejection under 35 U.S.C. 103(a). See MPEP § 706.02(l)(1) and § 706.02(l)(2). .

With regard to claim 22, Intel Corporation fail to teach a USB connector, matable with a corresponding USB connector of the computer system, at which at least one additional USB data signal and at least one USB power signal generated by the computer system are received, wherein each of the additional USB data signal and USB power signal is routed to one or more of the at least one USB port.

Lelong et al. teach a USB connector (Figure 2, item 103), matable with a corresponding USB connector of the computer system (Figure 2, labeled "USB header"; Figure 1, item 15), at which at least one additional USB data signal and at least one

USB power signal generated by the computer system are received, wherein each of the additional USB data signal and USB power signal is routed to one or more of the at least one USB port (paragraph 39).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to incorporate the USB connector as taught by Lelong et al. into the expansion card of Intel Corporation. This would have been obvious in order to allow the USB ports provided on the expansion card to be controlled by a USB controller incorporated into the computer system motherboard.

With regard to claim 23, Intel Corporation implicitly teach the additional limitation wherein the expansion card further comprises:

A power connector, matable with a corresponding power connector of the computer system, through which the power signal is received (Intel Corporation teach an AGP add-in card, which contains a power connector in the slot connector; namely pins A1, B2, B3, B5, B9, A9, and several others that provide voltages).

Examiner takes official notice that it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to route the power signals to the at least one or more of the USB-Plus-Power ports. This would have been obvious since without doing so, the USB-Plus-Power port would not provide power to the attached device.

With regard to claim 24, Intel Corporation implicitly teaches the additional limitation wherein the additional power signal is a 12VDC power signal. This is evidenced by the page 231, Table 5-2 which lists a 12VDC power signal on pin A1.

With regard to claim 26, USBIF teaches the additional limitation of a 24VDC power signal routed to one or more of the at least one USB-Plus-Power ports (page 8, section 3.1), but fail to explicitly teach a circuit configured to convert the 12VDC power signal to a 24VDC power signal. Examiner takes official notice that voltage-doubling circuits are old, and well known in this art. Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to utilize a voltage-doubling circuit in the expansion card of Intel Corporation, and USBIF for the purpose of providing the 24VDC in a USB port as required by the USB-Plus-Power specification.

* * *

Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Intel Corporation, in view of USBIF, and further in view of Espenshade et al.

With regard to claim 25, Intel Corporation, and USBIF fail to teach the expansion card further comprising at least one circuit each associated with one of the at least one USB port, wherein each circuit performs signal conditioning operations on signals to be provided at its associated USB-Plus-Power port.

Espenshade et al. teach a USB connector that comprises a circuit that performs signal conditioning operations on signals to be provided at its associated USB-Plus-Power port (column 2, lines 9 – 15).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to include the signal conditioning USB connector of Espenshade et al. in the expansion card of Intel Corporation, and USBIF. This would have been obvious since Espenshade et al. teach that the signal conditioning components within their USB connector eliminates undesirable extraneous signals such as high frequency noises (column 4, lines 25 – 28).

Allowable Subject Matter

Claims 9, 10, 18, and 19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew D. Spittle whose telephone number is (571) 272-2467. The examiner can normally be reached on Monday - Friday, 8 - 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on 571-272-3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MDS

Khanh Dang
Primary Examiner